

Technology Development for Building Flexible Silicon Functional Fibres

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Abstract

Most of everyday clothing consists of textile fibres woven together to produce a fabric. Their primary purpose is structural and aesthetic. Fibres can have added functionality by the integration of computing power into the material that forms them. The purpose of the 'fibre computing' concept is to integrate this new dimension of functionality into fibres, thus turning everyday clothing objects into intelligent artefacts [1]

1. Introduction

The vision of integrating computing power into clothes or other entities of that kind, is that "eventually, whole computers might be made from materials people are comfortable wearing" [2]. Lind et.al. similarly stated that "it is only appropriate that the field of textiles takes the next evolutionary step towards integrating textiles and computers by designing and producing a weavable computer that is also wearable like any other textiles" [3]. These ideas foresee the seamless integration/embedding of computational functions into textiles in a natural way without changing the original function of the entity. In order to make a computer "wearable", it should dissociate the ordinary textile (e.g. clothing) into its basic components and seek a way of embedding or integrating the computing power into these units.

The concept of "Fiber Computing" is to embed the basic unit of computation, the transistor, into fibers that make up the garment. These transistors then may be connected to form inverters, gates and higher level circuits. The goal of fibre computing [4] is to turn existing "bricks around the body" into a comfortable, flexible and wearable textile form. With the successful integration of these fibers into clothes, the infrastructure for making a computer "truly weavable" will be initiated.

Integrating electronics into ubiquitous or wearable systems started with packaged integrated electronic components (ICs) interconnected with each other on a rigid or flexible printed circuit board [5,6]. Previous and current state of the art work [7,8] in integrating electronics into wearable systems comprises of previously packaged integrated electronic

components, interconnected with each other by means of conductive fibers [9] and hermetically sealed by protective material/casing.

A new concept will be discussed in this paper, which has the potential to change the way advanced circuits and systems are designed and fabricated in the future. This aim is to make large flexible integrated systems for wearable applications by building functional fibres with single crystal silicon transistors at its core [10]. Two different configurations were examined for the fabrication of flexible intelligent fibres, the production of a passive fibre and the SOI technique. Figure 1 illustrates the passive fibre configuration.

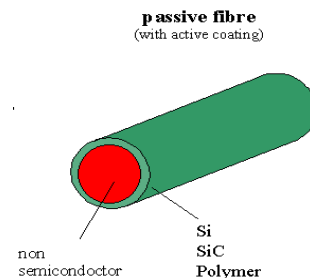


Figure 1 –The Passive Fibre Configuration.

Much work has been done in the examination of the strength of silicon microstructures and it has been established that silicon structures become extremely flexible when sufficiently thin [11-13].

The other approach to this novel technology that enables the fabrication of functional flexible silicon fibers has been developed and is termed the SOI technique. The concept involves building a circuit in silicon on insulator material (SOI) [14] and releasing the circuit by under-cutting the sacrificial silicon dioxide layer by means of a chemical wet etch process. This leaves the fiber completely free to move and to be extracted onto a flexible support structure. A functional device based on this experimental approach has already been fabricated in the form of a working flexible diode.

Subsequent active device circuits have been designed and fabricated. This technique has the potential to provide a planar technology that can manufacture extremely powerful circuits

and systems in long narrow fibres, which can be woven into fabrics.

2. Fiber Extrusion

One approach to creating circuits on a fibre is the fabrication of a flexible material (SiO_2) and coating this with an active silicon layer by means of a PVD process. All the IC processing is to be performed on this outer active silicon layer. The fabrication of these fibres is done by means of an extrusion technology. A mixture of fine ceramic powder and organic additives is pushed through a small orifice by a screw, with the resulting fibre sintered to obtain a ceramic fibre. A schematic illustration of this process is shown in Figure 2. A big advantage of this process is that a variety of desired cross-sectional geometries and even hollow fibers can be realized [15].

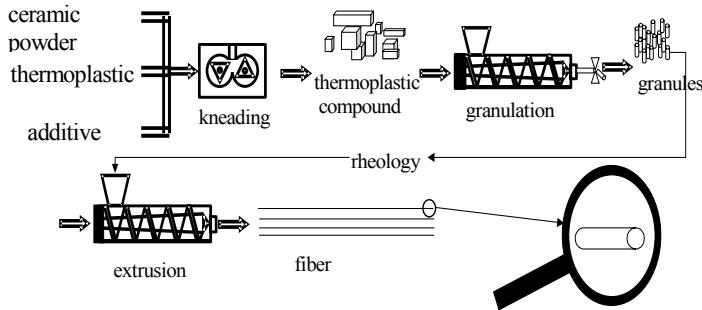


Figure 2. Concept of the inorganic fibre extrusion process used at EMPA

SiO_2 -fibres sintered at 1100°C exhibited an amorphous glass structure. Crystallization at the fibre surfaces was seen to occur at higher sintering temperatures. Some glass fibers were coated with a thin layer of silicon by using a PVD process. Figure 3 shows a SEM picture of the coated fibers, which have a glass core diameter of $125\mu\text{m}$ and a $1\mu\text{m}$ thick active polysilicon coating layer. These fibres have a tensile strength of 70 GPa. Figure 4. Illustrates the flexible nature of these extruded fibres. As one method for processing circuits in fibre form, the extruded fibres may also be used as a support structure for the SOI fibres discussed in section 3.

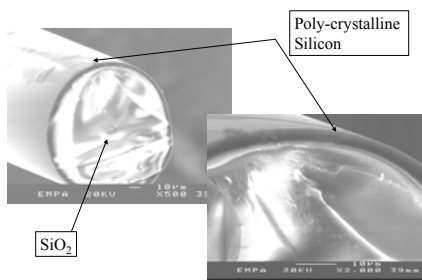


Figure 3. Si-coated silicon oxide glass fiber

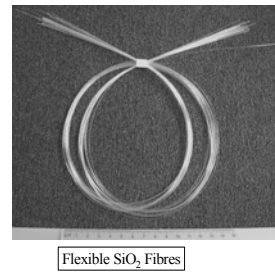


Figure 4. Flexibility of Si-coated silicon oxide glass fiber

3. SOI Technology Development

A novel technology that enables the fabrication of functional flexible silicon fibres using conventional planar processing has been developed. A prototype demonstration of functionality has been made i.e. a p-n junction has been fabricated on a fibre. Figure 5 shows the diode fibre after release from the handle wafer, Figures 6 and 7 show the diode characteristic curves for before and after release.



Figure 5. Free-standing fibre

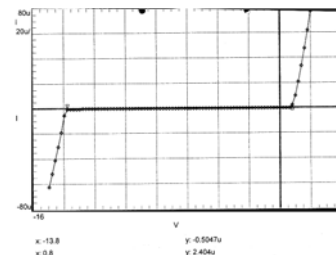


Figure 6. Diode Characteristics Before Release

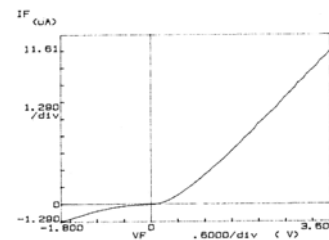


Figure 7. Diode Characteristics After Release

3.1 Active Device Circuit Design

The ring oscillator is a standard circuit for delay measurement. The layout consists of an odd number of inverters (see figure 8) connected in a circular chain. For the purpose of this experiment a 679-stage ring oscillator was designed.

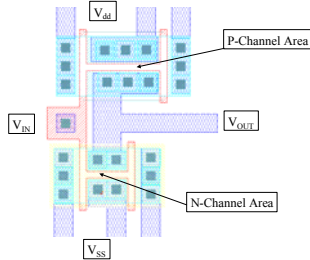


Figure 8. Design Layout of the SOI Inverter

The mechanical flexibility required to integrate the circuit into a wearable artifact is a key issue. This is resolved initially by using a polyamide flex material instead of BPSG oxide as the interlayer dielectric in the circuit. Secondly by using polyamide as a passivation layer covering the circuit, it will act as a support structure holding all the individual silicon islands along the circuit together after release from the handle wafer.

There are three different types of ring oscillator designed, all with different numbers of chains of inverters involved, with each chain consisting of 679 stages. An Example of the different ring oscillator designs is illustrated in figure 9.

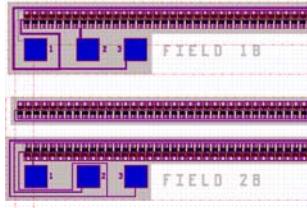


Figure 9. Design layout of a ring oscillator

3.2 Active Device Circuit Fabrication

The ring oscillator is fabricated on single crystal silicon SOI type structure wafers. The handle wafer is 525 μ m thick with a 4000 \AA buried oxide layer and a 3400 \AA thick silicon device layer. A brief outline of the fabrication process can be seen in figure 10.

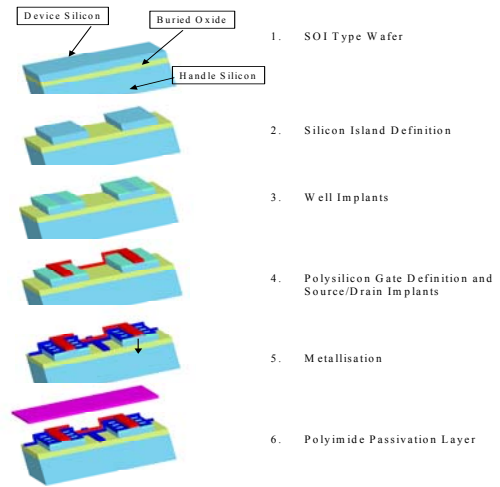


Figure 10. Active Device Circuit Process Flow

Firstly the silicon islands are defined by means of plasma etch and the gate oxidation and well implants follow. A 3500 \AA layer of polysilicon is deposited and patterned to create the gate. This is followed by source/drain implants of phosphorous ($5e14@60\text{KeV}$) and boron ($2e11@70\text{KeV}$). The contact stage is a 3 μ m patterned layer of polyamide used to increase the flexibility of the circuit after release from the handle wafer. A 6000 \AA layer of Al1%Si metal is deposited and patterned to create the interconnect between silicon islands. Finally a polyamide passivation layer is deposited and patterned over the circuit to increase the flexibility and overall mechanical robustness of the circuit.

The final circuit can be seen in figure 11. These circuits are release from the handle wafer to create a free-standing functional fibre.

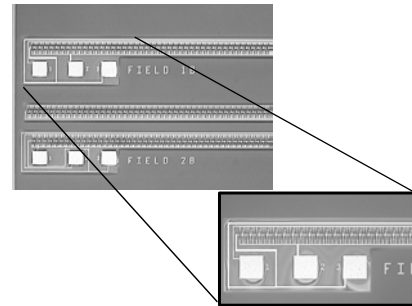


Figure 11. Final circuit after 1.5 μ m CMOS processing

3.3 Circuit Evaluation

Figure 12. Illustrates the waveform of a single strip 679 stage ring oscillator at wafer level. As can be seen the period of oscillation is approximately 25 μ sec, which is equivalent to a frequency of 40 KHz.

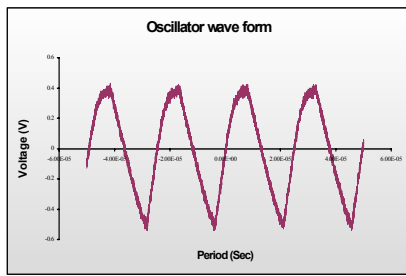


Figure 12. Waveform of a 697-stage ring oscillator

3.4 Current Work

Current work involves the release of the active fibers from the handle wafer and the subsequent testing of the free-standing active device circuits. The individual fibers will be released from the handle wafer by dry plasma etching the bulk silicon through the back of the wafer and using the thin oxide layer as an etch stop (see figure 13). These will then be laser cut from the oxide and characterised mechanically to observe the effects of bending on the circuits.

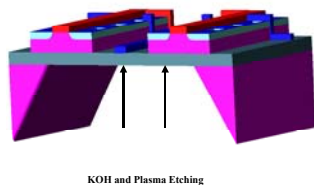


Figure 13. Circuit release process

3.5 Fibre Processing Issues

There are two main issues involved with processing on extruded fibres. Initially, there is the problem of securing the fibres for subsequent processing. The other issue for processing circuits on the passive fibre structures is the depth of field or focus latitude for the features printed. Advanced lithography systems have very small depths of field to allow for very small feature size resolution. Since the fiber is not flat this will pose an extra degree of complexity for the design rules. A typical optical lithography system has a depth of focus of $\pm 1.0\mu\text{m}$ for $1\mu\text{m}$ features. This will mean that critical features will have to be designed in the centre of the fiber and less critical features towards the edges.

There are other issues involving the SOI structures such as handling and the release of the top silicon device from the handle wafer to create the free-standing functional fibre. Interconnection between the fibres and an outside power supply is also a key issue of concern. One method of connection is by means of a conductive adhesive material and flexible laminate.

4. Conclusion

The concept of flexible devices and the different approaches to developing fibre technology have been presented in this paper. The extrusion process for developing passive fibres and the issues involved, have been presented.

Flexible silicon fibers using the SOI technique have been fabricated and tested. A detailed description of the design and processing issues involved, have been described along with an electrical reliability evaluation of the fibres before undergoing the release process.

Acknowledgement

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